REMARKS/ARGUMENTS

Reconsideration of this application is respectfully requested.

The rejection of claims 1, 14, 21-23, 29, 38-42 and 45 under 35 U.S.C. §103 as allegedly being made "obvious" based on Tanisawa '778 in view of Iha '429 is respectfully traversed.

In a nutshell at the outset, neither of the cited references teaches or suggests any packaging layer. In particular, none of the structures described in either of the references (whether considered singly or in combination) provides a packaging layer addressing the problems and issues that are addressed by the applicant's packaging layer.

Amended claim 1 is believed to be patentably distinct from the prior art for at least the reasons discussed below. The added feature that the packaging layer is substantially continuous apart from at least one recess is based on the packaging layers shown and described in the specification, all of which are substantially continuous apart from one or more recesses for use in assembling component(s) thereinto. This allows the packaging layer to provide any one or more of the common functions of a packaging layer, including planarization, protection and support to the component(s) for handling and processing.

New claim 54 is believed to be patentably distinct in offering a packaging layer that will surround and protect a component or its interconnect structure. Claim 54 is based on un-amended claim 1 with the added feature of the recess *"having a perimeter which is substantially closed into which a protected optical component, or electrical interconnect structure therefor, is assembled"*. This added feature is again based on the packaging layers shown and described in the specification, all of which include one

or more recesses with closed perimeters for receiving and protecting components or their interconnect structures.

An amendment has been made to claim 1 to characterize the nature of the packaging layer as being substantially continuous except for one or more packaging recesses. Such a layer is a typical packaging layer in that it can, for example:

- provide physical protection and support
- provide strength in the assembly for handling purposes
- embed components
- avoid having to provide infill
- offer planarization.

The cited documents do not between them appear to disclose any layer really intended for packaging at all.

In Tanisawa, the Examiner refers to Figure 4 and, in particular, to an electrically insulating layer 33. This insulating layer 33, as well as providing an electrical function, is also used to position an optical semiconductor chip 5 accurately in a vertical direction as shown in Figure 4. This is to align it with an optical waveguide 8 on a secondary surface 3 of substrate 1.

The insulating layer 33 has no real packaging role in the sense intended in claim 1 since there are complete breaks or gaps in it, exposing the principal surface 2 of the substrate 1 at the front and back ends of the chip 5 as shown.

The alternative Tanisawa arrangement shown in Figure 6 emphasizes that there is absolutely no packaging function intended since, in Figure 6, the principal surface 2 of the substrate 1 itself replaces the insulating layer 33.

As discussed at the beginning of the applicant's specification, a packaging layer has a distinct function in protecting or supporting components for handling or further processing. A packaging layer might provide infill around structures, as shown in Figure 12 of the applicant's figures, where the packaging layer 200 provides infill around contact pads 1200, as well as completely protecting the surface of the substrate 100. Alternatively, a packaging layer might provide planarization, as provided by the layer 1700 in Figure 17 of the applicant's figures, which provides planarization with respect to an interconnect structure 1600 on the substrate 100.

In Tanisawa, the insulating layer 33 positioning the optical semiconductor chip 5 offers no protection in this way, whether mechanical or chemical, for handling or further processing. There is no passivation or planarization offered, or any other packaging function, just positioning for optical coupling so that the optical assembly will work, and electrical insulation.

Iha has been previously discussed. In Iha, a photosensitive borosilicate glass is disclosed for use as an insulating material, for example, for multilayer interconnected printed circuit board constructions. One could substitute the Iha insulating material for that of the insulating layer 33 of Tanisawa and one would still just have an insulating material with the secondary function of providing positioning for optical coupling. There would still be no disclosure of any packaging layer in the usual sense at all. More specifically, there would be no disclosure of the packaging layer of claims 1 or 54 since the insulating layer 33 of Tanisawa clearly has gaps in it right down to the substrate next to the component it is positioning, and does not provide a recess with a closed perimeter.

Given such fundamental deficiencies of both cited references with respect to independent claims 1 and 54, it is not necessary at this time to discuss additional deficiencies of this allegedly "obvious" combination of references with respect to other

aspects of the rejected claims. Suffice it to note that, as a matter of law, it is not possible to support even a *prima facie* case of "obviousness" unless the cited prior art at least teaches or suggests each and every feature of each rejected claim.

Accordingly, this entire application is now believed to be in allowable condition, and a formal notice to that effect is earnestly solicited.

Respectfully submitted,

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